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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,601	04/16/2004	Axel Brintzinger	2002 P 12364 US	1197

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EXAMINER	
THAI, LUAN C	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 11/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/826,601	BRINTZINGER ET AL.	
	Examiner	Art Unit	
	Luan Thai	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-25 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 16 April 2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/08/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "*a terminal of a second apparatus*", in claim 1; "*a printed circuit board*" in claims 2 and 21; "*a lead frame*" in claims 3 and 21; and "*separation corridors*" in claims 9-11, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 4-9, 12-17 and 21-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Farnworth (5,933,713) and Heo (5,908,317) separately.

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1, 2, 4-9, 12-17 and 21-25, Farnworth (see specifically figures 1, 2, 5-6, 14-17) disclose a method of manufacturing a module, the method comprising: providing a device (e.g., semiconductor wafer 20) that includes a connection area or 3D structure (e.g., solder

bumps 30/70) extending over a top surface of the device, applying a casting compound (42/76) over the top surface of the device so that the connection area protrudes through the casting compound (42/76), wherein the casting compound comprises silicon-based material, thermoplastic material or epoxy resin (Col. 6, lines 30+); and after applying a casting compound, electrically coupling the connection area to a terminal of a second apparatus (e.g., printed circuit board, Col. 7, lines 1+) by soldering, wherein separation corridors (92) between the chips on the wafer are exposed before the separating (see figures 16-17).

Regarding claims 1, 2, 4-9, 12-17 and 21-25, Heo (see specifically figures 3-7) disclose a method of manufacturing a module, the method comprising: providing a device (10) (e.g., a part of semiconductor wafer 70, see figure 6) that includes a connection area or 3D structure (e.g., chip bumps 20) extending over a top surface of the device, applying a casting compound (13) over the top surface of the device so that the connection area protrudes through the casting compound (13), wherein the casting compound comprises silicon-based material, thermoplastic material or epoxy resin (Col. 4, lines 18+); and after applying a casting compound, electrically coupling the connection area to a terminal of a second apparatus (e.g., printed circuit board 40, see figures 7A-7B) by soldering, wherein separation corridors between the chips on the wafer are exposed before the separating (see figure 6).

4. Claims 1, 2, 4-8, 12-17 and 21-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Stepniak et al. (6,916,684).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1, 2, 4-8, 12-17 and 21-25, Stepniak et al. (see specifically figures 1-3) disclose a method of manufacturing a module, the method comprising: providing a wafer (11) which comprises plurality of chips (10), wherein each of chips (10) including a connection area or 3D structure (e.g., solder balls 12) extending over a top surface of the device, dispensing a casting compound (18) over the top surface of the device (11) so that the connection area (12) protrudes through the casting compound (18), wherein the casting compound having thermal and mechanical properties compatible to silicon (Col. 4, lines 50+); and after applying a casting compound (18), electrically coupling the connection area to a terminal (28) of a second apparatus (e.g., printed circuit board 26, see figures 2-3).

5. Claims 1, 2, 4-8, and 12-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Hiatt et al. (6,673,649).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1, 2, 4-8, and 12-25, Hiatt et al. (see specifically figures 2-7) disclose a method of manufacturing a module, the method comprising: providing a device (130) including a connection area or 3D structure (e.g., solder balls 150) extending over a top surface of the device, dispensing a casting compound (160) over the top surface of the device (130) (figure 3B-3C), reducing a thickness of the casting compound (160) by thermal removal or etching (Col. 5, lines 66+, Col. 6, lines 2+) so that the connection area (150) protrudes through the casting compound (160) (see figure 3E), wherein the casting compound comprises silicon-based material, thermoplastic material or epoxy resin (Col. 5, lines 40+, Col. 7, lines 1+); and after

reducing the thickness of the casting compound (160), electrically coupling the connection area (150) to a terminal (122) of a second apparatus (e.g., printed circuit board 120, see figures 4-7).

6. Claims 1, 4-7, 12-17 and 21-25, are rejected under 35 U.S.C. 102(e) as being anticipated by Hsieh et al. (6,790,758).

Regarding claims 1, 4-7, 12-17 and 21-25, Hsieh et al. (see specifically figures 1-3) disclose a method of manufacturing a module, the method comprising: providing a device (200) including a connection area or 3D structure (e.g., solder bumps 210) extending over a top surface of the device, dispensing a casting compound (212) over the top surface of the device (200) (figures 2F, 2G) so that the connection area (210) protrudes through the casting compound (212), wherein the casting compound comprises silicon-based material, thermoplastic material or epoxy resin (Col. 3, lines 49+); electrically coupling the connection area (210) to a terminal (306) of a second apparatus (e.g., a substrate 300, see figure 3, or a printed circuit board 106, see figure 1, Col. 1, lines 44+ and lines 59+).

7. Claims 1-9, 12-17 and 21-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Storli (6,885,101).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1-9, 12-17 and 21-25, Storli (see figures 1-4) discloses a method of manufacturing a module, the method comprising: providing a device (10) comprising a wafer 12 including plurality of chip (20), each of chips (20) includes a connection area or 3D structure (e.g., solder bumps 70) extending over a top surface of the device, dispensing a casting compound (80) over the top surface of the device so that the connection area protrudes through

the casting compound (80), wherein the casting compound comprises silicon-based material, thermoplastic material or epoxy resin (Col. 6, lines 2+). Storli further discloses separation corridors (28) between the chips (110) before the separating (see figure 3B). Storli also discloses the device package, which includes the solder balls (70) being conventionally connected to a printed circuit board or a lead frame (Col. 1, lines 33+).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-9, 12-17 and 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Luo et al. (6,885,108) in view of Chakravorty (6,181,569).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1-9, 12-17 and 21-25, Luo et al. (see figures 1-12) disclose a method of manufacturing a module, the method comprising: providing a device (12) (see figures 1, 2, 5-12) that includes a connection area or 3D structure (e.g., solder bumps 18) extending over a top surface of the device, applying a casting compound (20) over the top surface of the device so that the connection area protrudes through the casting compound (20), wherein the casting compound comprises silicon-based material, thermoplastic material or epoxy resin (Col. 5, lines 6+) and is applied by dispensing, spraying or printing (Col. 5, lines 34). Luo et al. further disclose separation corridors (28) between the chips (12) on the wafer being exposed before the

separating (see figures 6 and 7A), and the casting compound being cooling down before separating the chips (Col. 7, lines 21+). Luo et al. Disclose the solder balls (18) being external terminal of the device package (12). However, Luo et al. do not explicitly teach the device package (12) electrically connected to a printed circuit board or a lead frame.

Chakravorty while related to a similar Chip-sized-package design teach the external bump electrodes of the device package being electrically connected to printed circuit board or lead frame for the device package functioning as intended (Col. 1, lines 12+). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that device package of Luo et al should be connected to a printed circuit board or a lead frame as taught by Chakravorty, in order for the device package to function as intended.

10. Claim 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Luo et al. (6,885,108) and Chakravorty (6,181,569) as applied to claim 9 above and further in view of Ha et al. (6,339,251).

Regarding claim 10, the proposed method of Luo et al. and Chakravorty disclose the limitations of the invention as detailed above except for a photolithographic process being used to expose the separation corridors or the scribe lines.

Using a photolithographic process to expose the separation corridors or the scribe lines on the wafer is commonly applied in semiconductor art as disclosed by Ha et al. (Col. 4, lines 14+). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to applied the photolithographic process to the proposed method of Luo et al. and Chakravorty in order to expose the separation corridors or the scribe lines on the wafer since photolithographic process is commonly applied in the art to expose the scribe lines as taught by Glenn et al.

11. Claim 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Luo et al. (6,885,108) and Chakravorty (6,181,569) as applied to claim 9 above and further in view of Glenn et al. (6,420,776).

Regarding claim 11, the proposed method of Luo et al. and Chakravorty disclose the limitations of the invention as detailed above except for a laser beam being used to expose the separation corridors or the scribe lines.

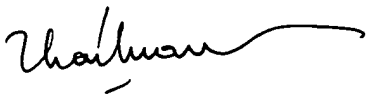
Using a laser beam to expose the separation corridors or the scribe lines on the wafer is commonly applied in semiconductor art as disclosed by Glenn et al. (Col. 5, lines 59+, Col. 7, lines 4+, Col. 8, lines 47+, Col. 10, lines 30+). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to applied the laser beam to the proposed method of Luo et al. and Chakravorty in order to expose the separation corridors or the scribe lines on the wafer since laser beam is commonly applied in the art to expose the scribe lines as taught by Glenn et al.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:30 AM - 5:00 PM, Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Luan Thai
Primary Examiner
Art Unit 2891
November 7, 2005